AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of physical circuit design comprising the steps of:

packing components of a circuit design that are dependent upon an architecture of the circuit design;

assigning initial locations to components of the circuit design;

clustering a plurality of components of the circuit design according to design constraints so as to leave white space in at least one circuit cluster; and

placing the components of the circuit design to minimize critical connections.

2. (Original) The method of claim 1, wherein said clustering step operates on components that are not dependent upon the architecture of the circuit design.

3. (Original) The method of claim 1, wherein said step of assigning initial locations is not timing driven.

4. (Previously Presented) The method of claim 1, said clustering step further comprising the step of combining slices that share control signals and clock sources to form a combined slice such that the total number of components of the combined slice does not exceed a threshold number of components.

5. (Original) The method of claim 1, further comprising:

declustering the circuit design; and

performing post-placement tasks on the declustered circuit design; and wherein said clustering step further comprising including slices in a configurable logic block if the total number of inputs and outputs of the resulting configurable logic block does not exceed a threshold number of inputs and outputs.

6. (Original) The method of claim 5, wherein the threshold number of inputs and outputs is less than the number of inputs and outputs that can physically be

accommodated by the configurable logic block so as to leave white space in the configurable logic block for post-placement circuit optimizations.

7. (Original) The method of claim 1, said clustering step further comprising the step of adding a slice to a configurable logic block if the slice has a critical attraction to a slice already included in the configurable logic block.

8. (Original) The method of claim 1, said clustering step further comprising the step of using fanout to determine which slice is included in a configurable logic block if more than one slice to be added to the configurable logic block has an equivalent critical attraction to a slice within the configurable logic block.

9. (Original) The method of claim 1, said clustering step further comprising the steps of:

(a) selecting a critical connection of the circuit design;

(b) identifying a first slice connected to the critical connection;

(c) if the first slice is not clustered, identifying a second slice having a most critical attraction to the first slice;

(d) including the second slice with the first slice in a configurable logic block if the total number of inputs and outputs of the resulting configurable logic block does not exceed a threshold number of inputs and outputs; and

(e) repeating steps (a), (b), (c), and (d) for further slices connected to the critical connection.

10. (Original) The method of claim 9, further comprising the step of repeating said steps (a)-(e) for further critical connections.

11. (Original) The method of claim 9, wherein the threshold number of inputs and outputs is less than the number of inputs and outputs that can physically be accommodated by the configurable logic block so as to leave white space in the configurable logic block for post-placement circuit optimizations.

12. (Withdrawn) A method of clustering a circuit design comprising the steps of:

(a) selecting a critical connection of the circuit design;

(b) identifying a first slice connected to the critical connection;

(c) if the first slice is not clustered, identifying a second slice having a most critical attraction to the first slice; and

(d) including the second slice with the first slice in a configurable logic block if the total number of inputs and outputs of the resulting configurable logic block does not exceed a threshold number of inputs and outputs.

13. (Withdrawn) The method of claim 12, further comprising:

(e) repeating steps (a), (b), (c), and (d) for further slices connected to the critical connection; and

(f) repeating said steps (a)-(e) for further critical connections.

14. (Withdrawn) The method of claim 12, said step (d) further comprising the step of combining slices that share control signals and clock sources such that the total number of components of the combined slice does not exceed a threshold number of components.

15. (Withdrawn) The method of claim 12, said step (d) further comprising the step of adding a slice to a configurable logic block if the slice has a critical attraction to a slice already included in the configurable logic block.

16. (Withdrawn) The method of claim 12, said step (d) further comprising the step of using fanout to determine which slice is included in the configurable logic block if more than one slice to be added to the configurable logic block each has an equivalent critical attraction to a slice within the configurable logic block.

17. (Withdrawn) The method of claim 12, wherein the threshold number of inputs and outputs is less than the number of inputs and outputs that can physically be

accommodated by the configurable logic block so as to leave white space in the configurable logic block for post-placement circuit optimizations.

18. (Currently Amended) A system for physical circuit design comprising:

means for packing components of a circuit design that are dependent upon an architecture of the circuit design;

means for assigning initial locations to each component of the circuit design;

means for clustering the components of the circuit design by combining slices and including slices into configurable logic blocks according to design constraints so as to leave white space in at least one circuit cluster;

means for placing the components of the circuit design to minimize critical connections;

means for declustering the circuit design; and

means for performing additional post-placement placer tasks on the declustered circuit design.

19. (Previously Presented) The system of claim 18, said means for clustering further comprising means for combining slices that share control signals and clock sources to form a combined slice such that the total number of components of the combined slice does not exceed a threshold number of components.

20. (Original) The system of claim 18, said means for clustering further comprising means for including slices in a configurable logic block if the total number of inputs and outputs of the resulting configurable logic block does not exceed a threshold number of inputs and outputs.

21. (Original) The system of claim 20, wherein the threshold number of inputs and outputs is less than the number of inputs and outputs that can physically be accommodated by the configurable logic block so as to leave white space in the configurable logic block for post-placement circuit optimizations.

22. (Original) The system of claim 18, said clustering means further comprising:

(a) means for selecting a critical connection of the circuit design;

(b) means for identifying a first slice connected to the critical connection;

(c) means for identifying a second slice having a most critical attraction to the first slice if the first slice is not clustered;

(d) means for including the second slice with the first slice in a configurable logic block if the total number of inputs and outputs of the resulting configurable logic block does not exceed a threshold number of inputs and outputs; and

(e) means for repeating steps (a), (b), (c), and (d) for further slices connected to the critical connection.

23. (Original) The system of claim 22, wherein the threshold number of inputs and outputs is less than the number of inputs and outputs that can physically be accommodated by the configurable logic block so as to leave white space in the configurable logic block for post-placement circuit optimizations.

24. (Withdrawn) A method of physical circuit design comprising the steps of:

packing components of a circuit design that are dependent upon an architecture of the circuit design;

performing initial non-timing driven placement of the components of the circuit design;

clustering two or more components of the circuit design according to design constraints, wherein a cluster of components comprises an unused region;

placing the components of the circuit design using time driven placement;

declustering the circuit design; and

performing post-placement placer tasks on the declustered circuit design.

25. (Withdrawn) The method of claim 24 wherein the unused region comprises white space.

26. (Withdrawn) The method of claim 24 wherein a criteria for selecting a component for clustering comprises a criticality of a connection of the component with a clustered component.

27. (Withdrawn) The method of claim 26 wherein the criticality of the connection comprises a slack of the connection.

28. (Withdrawn) The method of claim 24 wherein a criteria for selecting a component for clustering comprises a critical attraction of the component.